

GENERAL DESCRIPTION

The 4290 is a complete operating system for multiwire drift chamber data-handling. The System, organized as a sub-system of CAMAC accepts differential ECL signals from chamber preamplifiers-discriminators such as the LeCroy Model 2735A.

Up to 23 Model 4291B 32 Channel Time Digitizer modules (736 wires) can be housed in a dedicated, standard CAMAC crate with a Drift Chamber TDC Controller, Model 4298, occupying the controller position (stations 24 and 25) of the crate. The Crate Controller acts as a fast data readout preprocessor, rejecting unwanted zero or full scale values during data-taking. Valid data are dumped via a fast bi-directional DATABUS into a parallel access, 4K x 16-bit memory housed in a DATABUS Interface module, Model 4299. The Interface obeys conventional CAMAC protocol and is therefore to be located in a crate on the data acquisition branch. Its large capacity allows buffering of more than one event on long-spill machines, and it also offers the advantage of concentrating a large amount of valid data in a single CAMAC crate for later microprocessor pre-analysis.

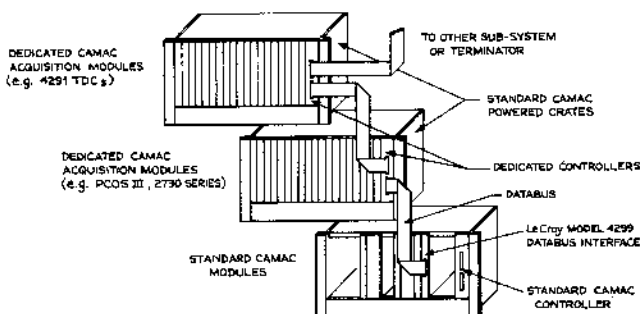
Each digitizer channel has the ability to be automatically trimmed so that all pedestals and slopes are set to identical values, thus eliminating the need to do computer corrections. To provide this and other test features, the 4298 Crate Controller acts as a programmable time mark generator for the test and calibration sequences. Alternating zero and full scale time signals are generated by the Controller, allowing each channel to "learn" the values of both trims. Initialized by an AUTOTRIM command at the 4299 Interface, the System can correct for all pedestal differences up to $\pm 5\%$ of the full scale time (e.g., ± 50 nsec for 1 μ sec full scale) caused by cabling and preamplifiers.

The full scale range can be continuously adjusted in each 4291 module from 500 nsec to 2 μ sec. Options for other ranges can be provided. The conversion time is 35 μ sec for 9-bit accuracy. Transfer time is 12.5 μ sec per "hit" 4291 module plus 0.5 μ sec per valid word (for 5-meter DATABUS).

Data may be recorded employing either a COMMON START or a COMMON STOP scheme. The former is uniquely suited to most synchronous accelerator configurations (PEP, PETRA, LEP, etc.) and the latter is suited to long-spill machines (SPS, FNAL, etc.)

A typical system configuration is illustrated on the cover. Its main components are the Model 4291B 32 Channel Time Digitizer, Model 4298 Dedicated Crate Controller, Model 4299 DATABUS Interface/Buffer, and Model 2735A Chamber Mounted Amplifier/Discriminator card.

SYSTEM CONFIGURATION



Dedicated CAMAC Model 4291B 32 Channel Drift Chamber Time Digitizer

The LeCroy Model 4291B is a single-width CAMAC module containing 32 time digitizers. Two 34-pin front-panel connectors (P1, P2), each accommodating 16 complementary inputs at ECL levels, allow use of twisted-pair ribbon cables from the discriminator outputs to the TDC's. The input impedance of the digitizers is 110 Ω .

Each digitizer consists of one LSI Custom Monolithic Model MTD110. This monolithic circuit has been expressly designed to provide excellent time resolution in applications where a large number of digitizers are required. It is a 9-bit plus overflow time-to-digital converter utilizing an analog time stretcher followed by a digital counter. An outstanding feature of this analog device is its self-calibration mode AUTOTRIMTM. This feature employs two sets of internal registers, DAC's, and digital comparators used to adjust both the offset and the slope of the analog ramp. In AUTOTRIM mode, a precision pulse source (in the 4298 Controller) generates a series of pulses that alternate between a pedestal count of two and a full scale count of 514 (overflow plus 2). The initial MTD110 registers are then appropriately updated causing perfect calibration to be achieved. The adjustment range corrects for unit-to-unit variations in manufacturing, as well as, slow temperature and/or voltage changes. The range of the offset adjusts is more than adequate for internal variations, and allows for the option of correcting for external cable and preamplifier variations. All of the active circuits are incorporated in a single, low-power, 18-pin DIP package, making it possible to achieve high accuracy and high density at low per-channel cost.

The 4291B offers either a COMMON START or COMMON STOP operating mode, user selected via the Model 4298 Crate Controller.

In the COMMON STOP mode, the Wire input to the differential receiver becomes the Start input. This begins the timing cycle, which is completed by receipt of an EXperiment Common trigger (derived from the event trigger) which generates a Stop. Subsequent Wire inputs before the trigger are each processed as another Start, just as if the System were quiescent. After the trigger pulse is received, the inputs are inhibited and the arrival time of the last Wire input pulse before the trigger (but within the full scale time range) is digitized and transferred to the 4298 Controller. This mode is ideal when a quality pretrigger is not available since the entire full scale time can be used as the trigger decision time.

In the COMMON START mode, the EXperiment Common trigger generates a Start used to initiate the timing cycle. Then the first Wire input received (during the full scale time) causes a Stop, and the timing cycle is completed. At the end of the full scale time, the conversion and transfer cycle is initiated.

In either mode, if a wire pulse is received during the full scale time, a HIT register will be set to provide a prompt indication of valid data. This HIT data is used internally to reduce readout time (only HIT modules are read out) and is available to the user via a rear panel connector for use in the higher level trigger logic.

TRIGGER DECISION LOGIC MODEL 4291B

In the Model 4291B, the hit registers are buffered and available in parallel on connector P3 located at the top rear end of the unit. The tristate TTL buffers, which are of negative-type logic, can be strobed via the ENABLE input of P3. A positive logic option is available upon request.

INPUT/OUTPUT SPECIFICATIONS

Hit Register Outputs: 32-bit parallel output provides low-power Schottky, low-true tristate output.

Output Enabled, No Hit: > 2.4 V at $+15$ mA max.

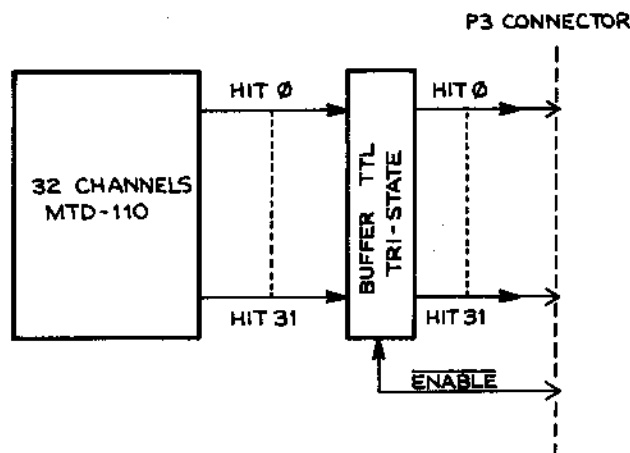
Output Enabled, Hit Present: < 0.5 V at -24 mA max.

Output Not Enabled: High impedance; ± 20 μ A.

Enable Input: High level disables (> 2 V, 0.1 mA max.). Low level enables (< 0.8 V, 0.4 mA max.). Enable time < 40 nsec. Data are available after the full scale time until reset.

P3 Connector: Rear panel 32-pin connector mates with same connectors as used on front panel. Detailed pin allocation is defined in the 4291B User Manual.

SPECIFICATIONS SUBJECT TO CHANGE



SPECIFICATIONS



Inputs:	32 ECL differential line receivers; 110 Ω input impedance; double-pulse resolution < 200 nsec in COMMON STOP mode (not applicable in COMMON START mode); 50 nsec minimum width.
Full Scale:	Continuously adjustable from 512 to 2048 nsec (1 nsec/count to 4 nsec/count) other ranges available on request.
Accuracy:	Gain accuracy within 0.1% with absolute accuracy within 1 count.
TDC Range:	9 bits plus overflow. Other options available on request.
Common Trigger:	Distributed by 4298 module via the CAMAC Dataway. In the COMMON START mode, the trigger must be supplied 200 nsec before the last expected wire pulse. In the COMMON STOP mode, the trigger must be supplied 200 nsec after the first expected wire pulse.
Pedestal Compensation:	External channel-to-channel variations in Wire input timing of up to $\pm 5\%$ of full scale time may be automatically compensated by the AUTOTRIM feature. (Requires that 4298 test pulses be supplied at the detector.)
Conversion and Transfer Time:	Approximately 35 μ sec plus 12 μ sec per "HIT" module plus 0.5 μ sec per valid word (for 5-meter DATABUS).
Reset (Fast Clear):	Distributed by 4298 module via the CAMAC Dataway. Resets TDC's and HIT registers in less than 300 nsec.
Readout Control:	Requires one Model 4298 module and one 4299 DATABUS Interface. All clocks, controls, test pulses, and data are bused via the CAMAC Dataway.
Trigger Decision Logic Outputs:	HIT pattern is available on upper rear connector P3 of CAMAC module. NOTE: A HIT is registered by any wire input occurring within the digitized time window plus a 10 to 20 percent extension on either end of this window.
Input Connectors:	Two lock and eject dual 17-pin headers. Mates with 3M 3414-6034, AMP 86987-1, or LeCroy CK/34. Pin assignments are listed in the User Manual. Cable should be 34 conductor twisted pair ribbon, SpectraStrip 455-248-34 or LeCroy DC2/34-L (cable with connectors) where L is the length in feet.
Current Requirements:	+ 24 V at 30 mA - 6 V at 900 mA + 6 V at 700 mA

SPECIFICATIONS SUBJECT TO CHANGE